

ADVANCED 4-HEAD  
 PLAY-BACK AND RECORD AMPLIFIER FOR VCR

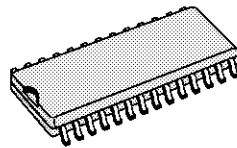
PRELIMINARY DATA

**PLAY-BACK MODE**

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 4 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAY-BACK OUTPUT WITHOUT AGC
- ONE PLAY-BACK OUTPUT INCLUDING AGC
- RECORD AMPLIFIER INHIBITION AND RECORD OUTPUT GROUNDED
- OUTPUT FOR TRACKING VIDEO INFORMATION (TRIV)
- SHORT PLAY/LONG PLAY ENVELOPE COMPARATOR WITH A SCHMIDT TRIGGER

**RECORD MODE**

- TWO INTEGRATED I/I CONVERTERS WITH ACCURATE CONTROL OF TRANSCONDUC-TANCE
- AUTOMATIC PLAY-BACK/RECORD SWITCHING BY SCANNING OF RECORD SUPPLY
- PLAY-BACK LOOP INHIBITION
- RECORD AMPLIFIERS WITH AUTOMATIC PROTECTION AGAINST SHORT CIRCUIT


 SO28 LARGE  
 (Plastic Micropackage)

ORDER CODE : TEA5706A

**PIN CONNECTIONS**

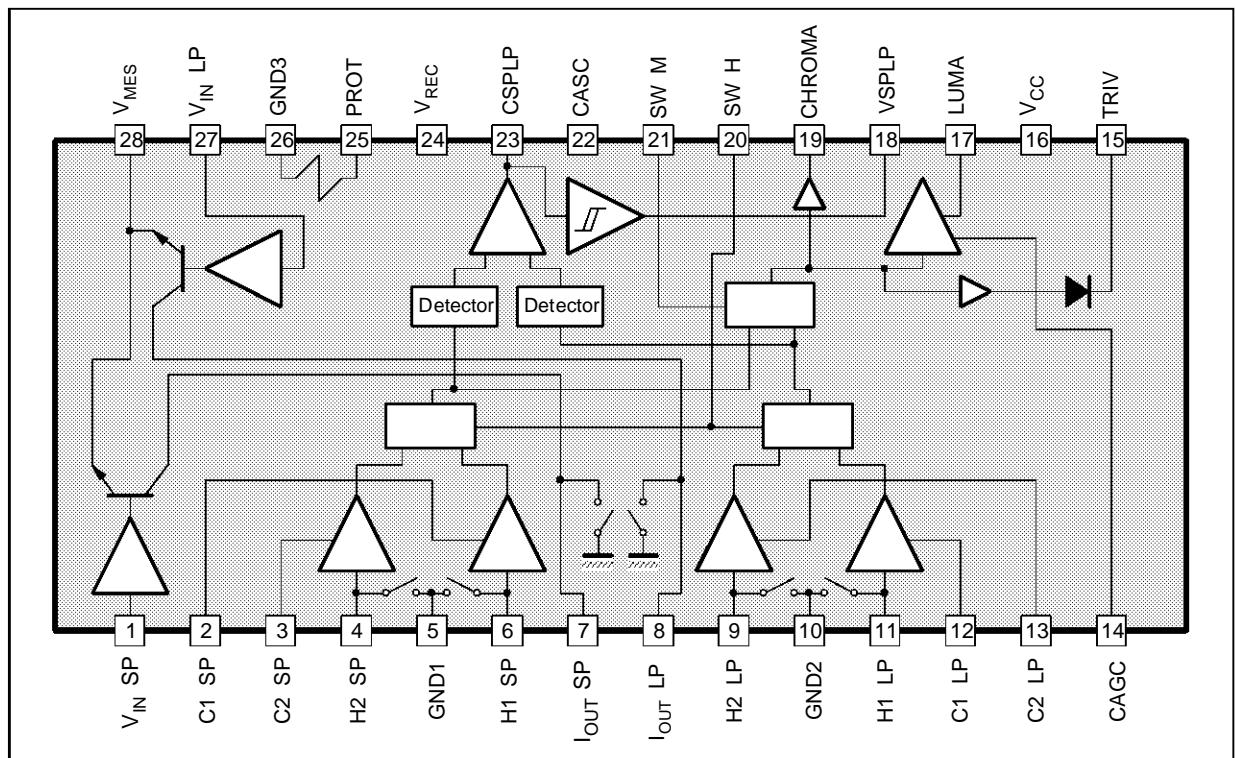
V <sub>IN</sub> -SP	1	28	V <sub>MES</sub>
C1-SP	2	27	V <sub>IN</sub> -LP
C2-SP	3	26	GND3
H2-SP	4	25	PROT
GND1	5	24	V <sub>REC</sub>
H1-SP	6	23	CSPLP
I <sub>OUT</sub> -SP	7	22	CCAS
I <sub>OUT</sub> -LP	8	21	SW-M
H2-LP	9	20	SW-H
GND2	10	19	CHROMA
H1-LP	11	18	VSPLP
C1-LP	12	17	LUMA
C2-LP	13	16	V <sub>CC</sub>
CAGC	14	15	TRIV

**DESCRIPTION**

The TEA5706A is an advanced four head record and play-back amplifier for VCR.

5706A01.EPS

## BLOCK DIAGRAM



5706A-02.EPS

## FUNCTIONAL DESCRIPTION

TEA5706A is intended for 4 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS and S-VHS applications (10MHz bandwidth).

High performance technology allows very low noise levels (current and voltage), which are frequency dependant in all the frequency range. In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5706A large capability to drive directly a coaxial cable in order to reduce number of external components.

Two play-back outputs are available : one, dedicated to Chroma processing, is a 60dB voltage amplifier output, the other, dedicated to Luma processing, has a constant AC output level of 200mV<sub>PP</sub> at 3.8MHz signal (phase is opposite to the chroma dedicated one).

A tracking information for video signal (TRIV) is Luma amplitude proportional and allows automatic phase correction.

An automatic scanning of record supply voltage permits TEA5706A automatically switching either in play-back or in record mode. The switching threshold voltage is fixed to a value which forbids

high current peaking through the heads.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for two recording heads, the DC current and the AC characteristics can be very precisely controlled with accurate external resistors. If recommended resistances are used, a  $\pm 5\%$  transconductance accuracy is guaranteed.

Feedback loop gains of SP channel and LP channel can be different.

The recording amplifiers include a protection system which protects the IC and the application board against overheating in case of short circuit on the recording transconductance components.

A particular feature is the SP/LP envelope comparator and detector. This system can be used in search mode, still mode, slow mode... The output signal is an output current feeding a capacitor (CSPLP) which is buffered through a schmidt trigger circuit to VSPLP. This output is high in record mode. By varying the capacitance on CSPLP a good compromise can be found between short delay time and spike free signal.

TEA5706A is fully protected against ESD.

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Power Supply Voltage	6	V
$V_{REC}$	Power Supply Voltage Record	15	V
$T_J$	Junction Temperature	+150	°C
$T_{oper}$	Operating Temperature	0, +70	°C

5706A-01.TBL

**THERMAL DATA**

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance (Typ.)	70	°C/W

5706A-02.TBL

**RECOMMENDED OPERATING CONDITIONS ( $T_{amb} = 25^{\circ}\text{C}$ )**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Power Supply Voltage	4.5	5	5.5	V
$V_{REC}$	Power Supply Voltage Record	4.75	9	12.6	V
CAGC	Capacitance at Pin CAGC	4.7			nF
CSPLP	Capacitance at Pin CSPLP		4.7		nF

5706A-03.TBL

**ELECTRICAL OPERATING CHARACTERISTICS ( $T_A = 25^{\circ}\text{C}$  unless otherwise specified)****Power Consumption**

Parameter	Play-Back		Record (1)	
	Typ.	Max.	Typ.	Max.
$V_{CC}$	60mA	75mA	40mA	55mA
$V_{REC}$	0mA	0mA	45mA	55mA
Total Consumption (2)	$V_{CC} = 5\text{V}, V_{REC} = 9\text{V}$	300mW		600mW
	$V_{CC} = 5.25\text{V}, V_{REC} = 9.45\text{V}$		375mW	
				750mW

5706A-04.TBL

**Notes :**

1.  $R_1 = 5.6\Omega$
2. Taking in account only the consumption through the IC.

A great care should be taken to the maximum power consumption :  $V_{REC}$  can be increased to 12.6V if the DC current flowing through the head is reduced. This can be done by increasing  $R_1$  value.  $V_{REC}$  can be reduced as long as voltage on Pins  $I_{out-SP}$ ,  $I_{out-LP}$  is not going under 1V (to forbid output stage saturation).

**Play-back Mode** $V_{CC} = 5\text{V}$ , no load on Pins CHROMA, LUMA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{CC1}$	Supply Current		45	60	75	mA
$V_{CC}$	Supply Voltage		4.75	5	5.25	V

**CHROMA OUTPUT (no AGC)**

$G_{PB}$	Pre-amplification Gain	Sinewave 600 kHz 400mV <sub>PP</sub> on output Input on Pin H1-SP or H2-SP, H1-LP or H2-LP	56	60	62	dB
$\Delta G_{PB1}$	Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2 in SP Mode	Sinewave 600kHz 0.4mV <sub>PP</sub> on inputs H1-SP and H2-SP			1.2	dB
$\Delta G_{PB2}$	Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2 in LP Mode	Sinewave 600kHz 0.4mV <sub>PP</sub> on inputs H1-LP and H2-LP			1.2	dB

5706A-05.TBL

## TEA5706A

---

### ELECTRICAL OPERATING CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified) (continued)

**Play-back Mode** ( $V_{CC} = 5\text{V}$ , no load on Pins CHROMA, LUMA)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CHROMA OUTPUT (no AGC) (continued)						
$e_N$	Equivalent Input Voltage Noise Level	Input grounded via switching transistor on Pins H1-SP, H2-SP, H1-LP, H2-LP, $f = 600\text{kHz}$		0.6	0.85	$\text{nV}/\sqrt{\text{Hz}}$
$i_N$	Equivalent Input Current Noise	Pins H1-SP, H2-SP, H1-LP, H2-LP		2	2.8	$\text{pA}/\sqrt{\text{Hz}}$
CRT	Crosstalk	Sinewave 3.8MHz $400\mu\text{V}_{PP}$ , All switches combined			-40	$\text{dB}$
$F_{LCPB1}$ $F_{HCPB1}$	Bandwidth Cut-off Frequency	-3dB attenuation $50\Omega$ in parallel on the input, 0dB at $600\text{kHz}$ Low High		8		$0.1$ $\text{MHz}/\text{MHz}$
$C_{IN}$	Input Capacitance Pins H1-SP, H2-SP, H1-LP, H2-LP	At 5MHz		30	40	$\text{pF}$
$R_{IN}$	Pre-amplifier Input Resistance Pins H1-SP, H2-SP, H1-LP, H2-LP	At 3.8MHz	400	600	900	$\Omega$
$Z_{CPB}$	Output Impedance Pin CHROMA	Sinus wave $600\text{kHz}$ $400\mu\text{V}_{PP}$ on input		30	50	$\Omega$
$V_{CPB}$	DC Level at Play-back Output on Pin CHROMA			1.5	1.9	$2.5$ $\text{V}$
$\Delta V_{CPBS}$ $\Delta V_{CPBL}$	Head Switch Offset Pin CHROMA				100 100	$\text{mV}/\text{mV}$
$SH_{PB1}$	Second Harmonic Play-back Output Pin CHROMA	Sinus wave 3.8MHz $400\mu\text{V}_{PP}$ on input with load $500\Omega//100\text{pF}$		-45	-40	$\text{dB}$

### LUMA OUTPUT (with AGC)

$Z_{LPB}$	Output Impedance	DC		30	50	$\Omega$
$V_{DCPB2}$	DC Level		0.8	1.4	2	$\text{V}$
$F_{LCPB2}$ $F_{HCPB2}$	Bandwidth Cut-off Frequency	-3dB attenuation $50\Omega$ in parallel on the input, AGC locked, 0dB at 3.8MHz Low High		10 12	0.1	$\text{MHz}/\text{MHz}$
$V_{LPB}$	Output Amplitude	Input signal $200\mu\text{V}_{PP}$ at 3.8MHz on Pins H1-SP, H2-SP, H1-LP, H2-LP	140	200	270	$\text{mV}_{PP}$
$\Delta V_{LPB}$	AGC Control Sensitivity	Input signal $200\mu\text{V}_{PP}$ at +6dB or -5dB on Pins H1-SP, H2-SP, H1-LP, H2-LP	-2		+1	$\text{dB}$
$SH_{PB2}$	Second Harmonic Play-back Output	Input Signal 3.8MHz $400\mu\text{V}_{PP}$ on Pins H1-SP, H2-SP, H1-LP, H2-LP with load $500\Omega//100\text{pF}$		-42	-35	$\text{dB}$

### CAGC

I+	Positive Output Current	Input Signal 3.8MHz $200\mu\text{V}_{PP}$ on H1-SP	15	30	45	$\mu\text{A}$
I-	Negative Output Current	Input Signal 3.8MHz $200\mu\text{V}_{PP}$ on H1-SP	-45	-30	-15	$\mu\text{A}$

### TRIV

R-TRIV	Downloading Resistance		20	40	80	$\text{k}\Omega$
$V_{TRIV1}$ $V_{TRIV3}$ $V_{TRIV4}$ $V_{TRIV5}$	Output Level	$V_{CHROMA} = 0\text{mV}_{PP}$ $V_{CHROMA} = 400\text{mV}_{PP}$ at 4.5MHz $V_{CHROMA} = 600\text{mV}_{PP}$ at 4.5MHz $V_{CHROMA} = 800\text{mV}_{PP}$ at 4.5MHz	0 2.6 3.3 3.6	3 3.4 3.7 4.2	1.2 3.4 4.1 4.5	$\text{V}$ $\text{V}$ $\text{V}$ $\text{V}$
$G_{TRIV1}$ $G_{TRIV2}$	Gain	$V_{CHROMA} = 0\text{mV}_{PP}, 400\text{mV}_{PP}$ at 4.5MHz $V_{CHROMA} = 400\text{mV}_{PP}, 600\text{mV}_{PP}$ at 4.5MHz		7.5 3.5		$\text{V}/\text{V}_{PP}$ $\text{V}/\text{V}_{PP}$

5706A-06.TBL

**ELECTRICAL OPERATING CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise specified) (continued)  
**Play-back Mode** ( $V_{CC} = 5\text{V}$ , no load on Pins CHROMA, LUMA)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>SP/LP ENVELOPE DETECTOR</b>						
$I_{DET+}$	Current Output on Pin CSPLP	200 $\mu\text{V}_{PP}$ on Pins H1-SP or H2-SP	25	50	75	$\mu\text{A}$
$I_{DET-}$	Current Output on Pin CSPLP	200 $\mu\text{V}_{PP}$ on Pins H1-LP or H2-LP	-75	-50	-25	$\mu\text{A}$
$V_{DETH}$	Sensitivity 1 on Pin CSPLP	50 $\mu\text{V}_{PP}$ to 600 $\mu\text{V}_{PP}$ on SP, LP short circuited	4	4.5	5	V
$V_{DETL}$	Sensitivity 2 on Pin CSPLP	50 $\mu\text{V}_{PP}$ to 600 $\mu\text{V}_{PP}$ on LP, SP short circuited	0	0.5	1	V
$V_{TH}$	Upper Threshold on Pin VSPLP	Scanning through Pin CSPLP		3.33		V
$V_{TL}$	Lower Threshold on Pin VSPLP	Scanning through Pin CSPLP		1.66		V
$R_{OH}$ $R_{OL}$	Output Resistance on Pin VSPLP	Output high Output low	7.5 1.5	12.5 2.5	17.5 3.5	$\text{k}\Omega$ $\text{k}\Omega$

5706A-07.TBL

**Record Mode** $V_{REC} = 9\text{V}$ ,  $V_{CC} = 5\text{V}$ , Load resistor  $50\Omega$  on Pin  $I_{OUT-SP}$ ,  $I_{OUT-LP}$ Transconductance network defined by :  $R_1 = 5.6\Omega$ , 1% Pins PROT/ $V_{MES}$  $R_2\text{-SP} = 2\text{k}\Omega$ , 1% Pins  $V_{MES}/V_{IN-SP}$  $R_2\text{-LP} = 1.5\text{k}\Omega$ , 1% Pins  $V_{MES}/V_{IN-SP}$  $R_3\text{-SP} = 1.5\text{k}\Omega$ , 1% Pin  $V_{IN-SP}$  $R_3\text{-LP} = 1.5\text{k}\Omega$ , 1% Pin  $V_{IN-LP}$ 

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{REC}$ $I_{CC2}$	Current Supply	$V_{REC} = 9\text{V}$ $V_{CC} = 5\text{V}$		45 40	55 55	mA mA
$I_{max}$	Max. Record Current on SP or LP Current Amplifier	3.8MHz	65			$\text{mA}_{PP}$
TR	Transconductance	$V_{IN-SP} = 300\text{mV}_{PP}$ $V_{IN-LP} = 300\text{mV}_{PP}$	180 150	230 180	280 210	$\text{mA/V}$ $\text{mA/V}$
SH <sub>REC</sub>	Second Harmonic	Output Current, 30mA <sub>PP</sub> at 3.8MHz at Pin $I_{OUT-SP}$ at Pin $I_{OUT-LP}$		-50 -50	-38 -38	dB dB
$F_{LCRSP}$ $F_{HCRSP}$	Bandwidth Cut-off Frequency Pin $I_{OUT-SP}$	-3dB attenuation, 0dB at 3.8MHz Output current 30mA <sub>PP</sub> Low High			0.1	MHz MHz
10						
V <sub>SPLP</sub>	DC Level at Pins CSPLP and VSPLP		4			V
$F_{LCRLP}$ $F_{HCRLP}$	Bandwidth Cut-off Frequency Pin $I_{OUT-LP}$	-3dB attenuation, 0dB at 3.8MHz Output current 30mA <sub>PP</sub> Low High			0.1	MHz MHz
10						
I <sub>PROT</sub>	Maximum Input Current on Pin PROT	5V on Pin $V_{MES}$	150	250	400	mA
V <sub>SAT</sub>	Maximum Saturation Voltage on Pin $V_{MES}$	Input current 80mA		50	150	mV
R <sub>VINLP</sub> R <sub>VINSP</sub>	Input Resistance on Pins $V_{IN-LP}$ , $V_{IN-SP}$	Equivalent value of R3 resistor	500	700	900	$\Omega$

5706A-08.TBL

## TEA5706A

### ELECTRICAL OPERATING CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified) (continued)

#### Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{SWHH}$	Head Selection Pin SW-H	Head number 1 in SP mode, 2 in LP mode (high level)	2.4		$V_{CC}$	V
$V_{SWHL}$		Head number 2 in SP mode, 1 in LP mode (low level)	0		1.5	V
$I_{SWHH}$		Input current (high level)		20	50	$\mu\text{A}$
$I_{SWHL}$		Output current (low level)		20	50	$\mu\text{A}$
$V_{SWMH}$	Mode Selection Pin SW-M (Record mode and play-back mode)	LP Mode (high level)	2.4		5	V
$V_{SWML}$		SP mode (low level)	0		1.5	V
$I_{SWMH}$		Input current (high level)		20	50	$\mu\text{A}$
$I_{SWML}$		Output current (low level)		20	50	$\mu\text{A}$
$t_{ON}$	Selection Pin SW-H or SW-M Transient Response	Delay time selection ON (output signal appears on Pin CHROMA)		250	1000	ns
$t_{OFF}$		Delay time selection OFF (output signal disappears on Pin CHROMA)		250	1000	ns
$V_{TH1}$	Inhibition Threshold for Switching from Play-back to record on Pin $V_{REC}$	$V_{CC} = 5\text{V}$	0.15	0.3	0.5	V
$V_{TH2}$	Inhibition Threshold Hysteresis for Switching from Record to Play-back on Pin $V_{REC}$	$V_{CC} = 5\text{V}$		80		mV
$t_1$	Transient Response of Record Scanning on Pin $V_{REC}$	Delay from play-back to record (signal disappears on Pin CHROMA)		30		$\mu\text{s}$
$t_2$		Delay from record to play-back (signal appears on Pin CHROMA)		35*		ms
$t_3$		Delay from play-back to record (signal appears on Pin $I_{OUT-SP}, I_{OUT-LP}$ )		0.2		ms
$t_4$		Delay from record to play-back (signal disappears on Pin $I_{OUT-SP}, I_{OUT-LP}$ )		8*		ms

\* Depending on capacitance on Pin  $V_{REC}$ .

5706A-09.TBL

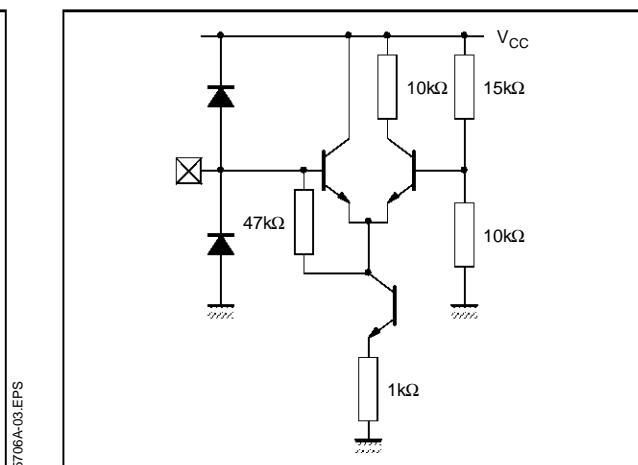
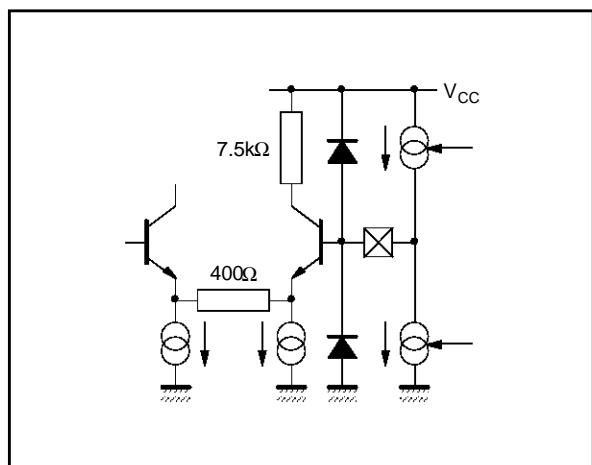
### Power Supply

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SVR	Supply Voltage Rejection	0.5mV <sub>PP</sub> on Pin $V_{CC}$ , 75 $\mu\text{V}_{PP}$ on Pin H1-SP, H2-SP, H1-LP, H2-LP, Measurement on Pin Chroma	15	20		dB

5706A-10.TBL

### INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

Pins : C1-SP, C2-SP, C1-LP, C2-LP

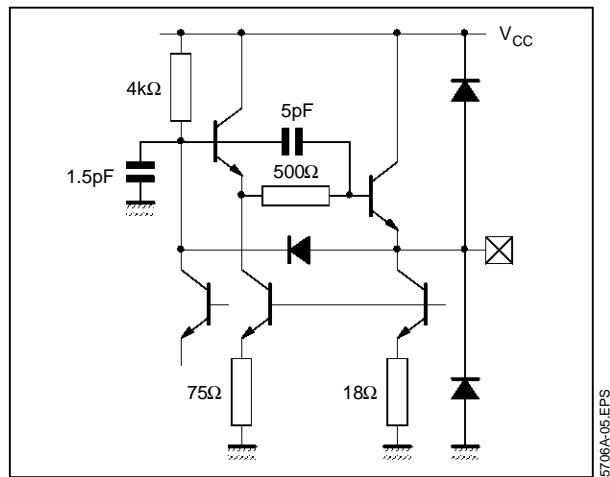


5706A-03.EPS

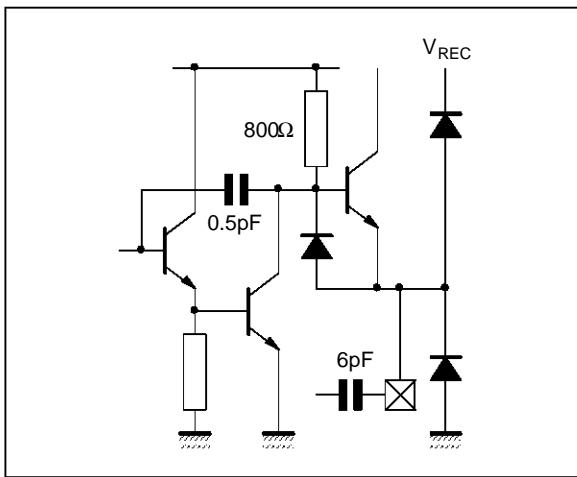
5706A-04.EPS

## INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

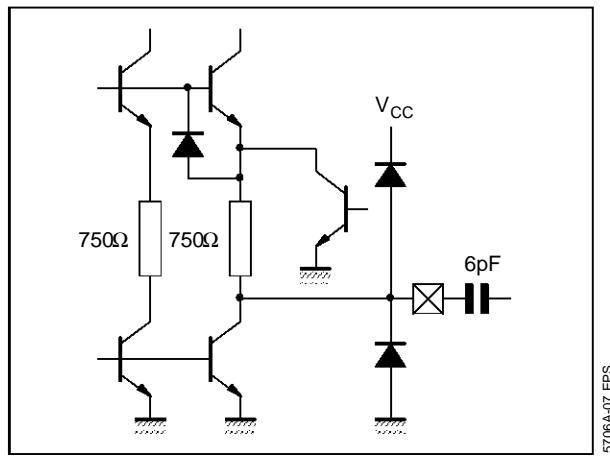
Pins : Chroma, Luma



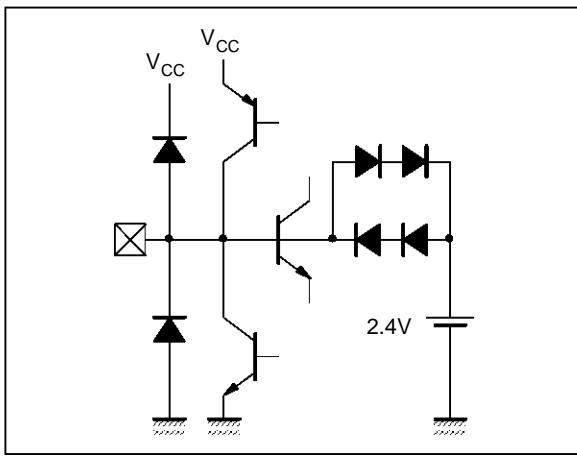
Pin : VMES



5706A-06.EPS

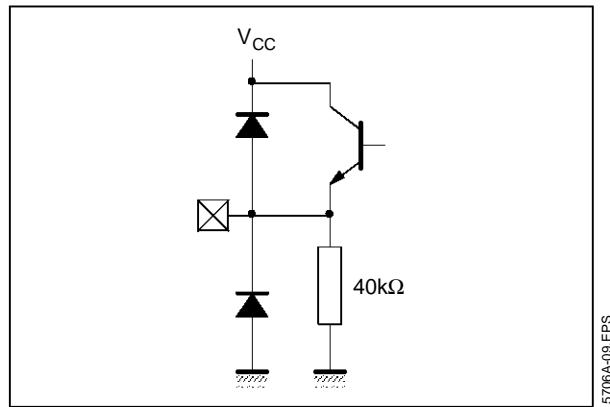
Pin : V<sub>IN-SP</sub>, V<sub>IN-LP</sub>

Pin : CAGC

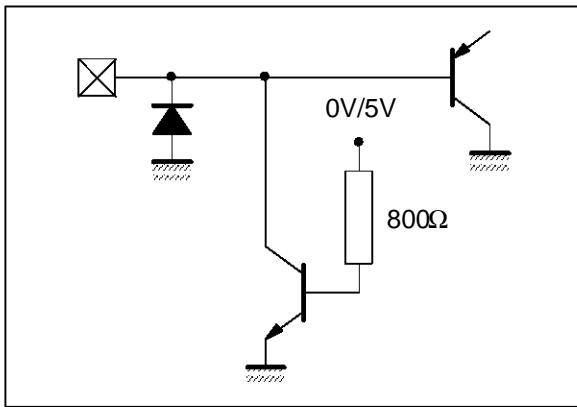


5706A-08.EPS

Pin : TRIV



Pin : PROT



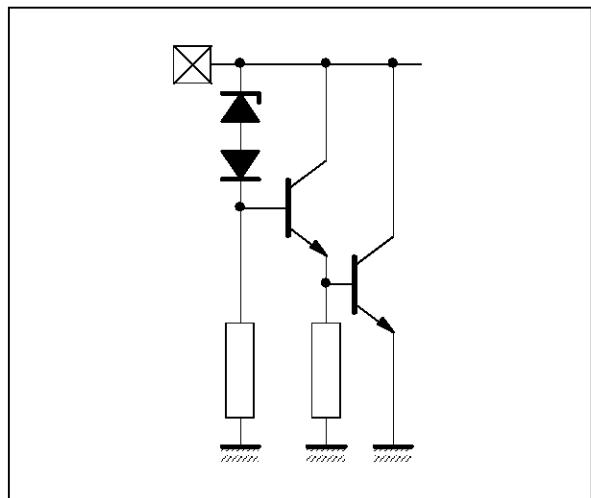
5706A-10.EPS

## TEA5706A

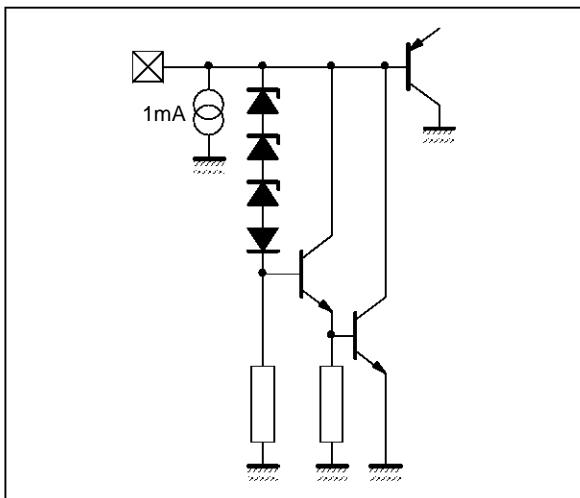
---

### INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

Pin : V<sub>CC</sub>

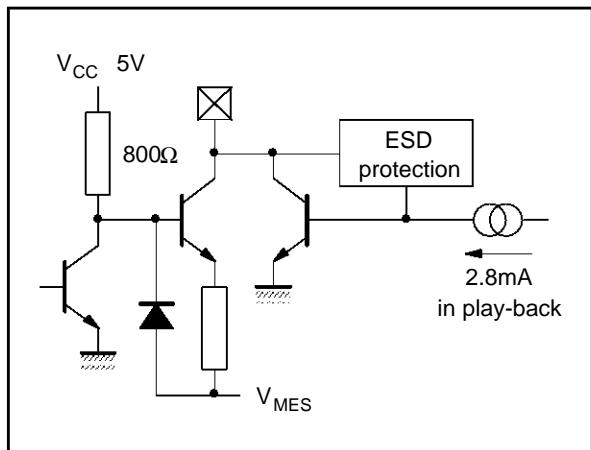


Pin : V<sub>REC</sub>



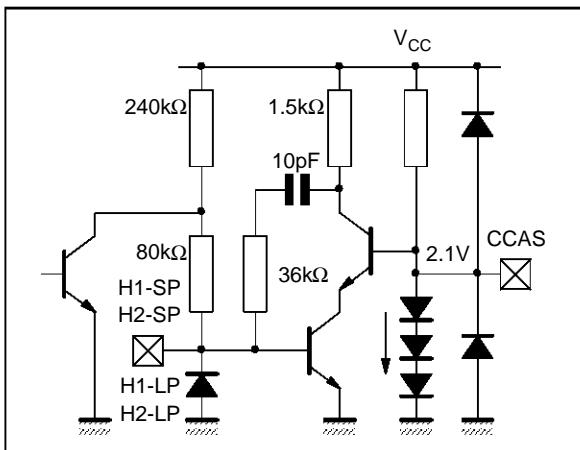
5706A-11.EPS

Pin : I<sub>OUT-SP</sub>, I<sub>OUT-LP</sub>



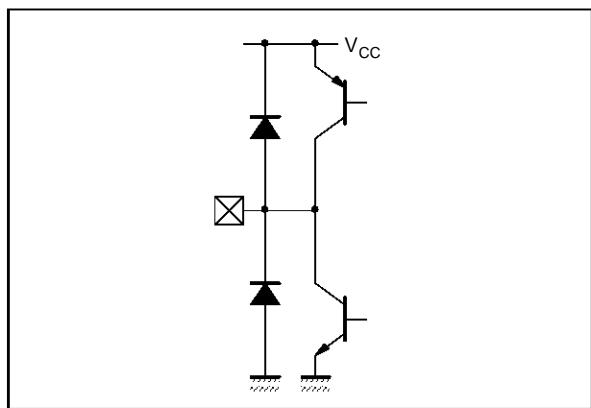
5706A-13.EPS

Pins : CCAS, H1-SP, H2-SP, H1-LP, H2-LP



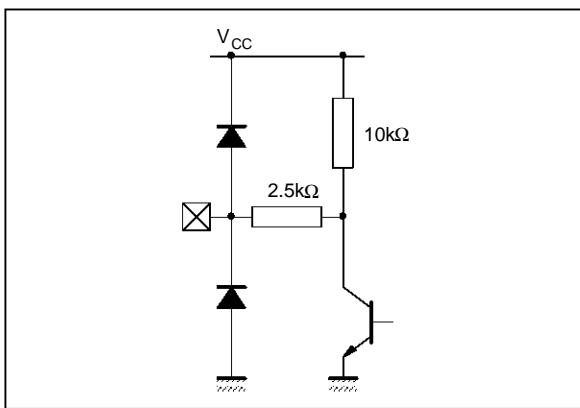
5706A-14.EPS

Pin : CSPLP



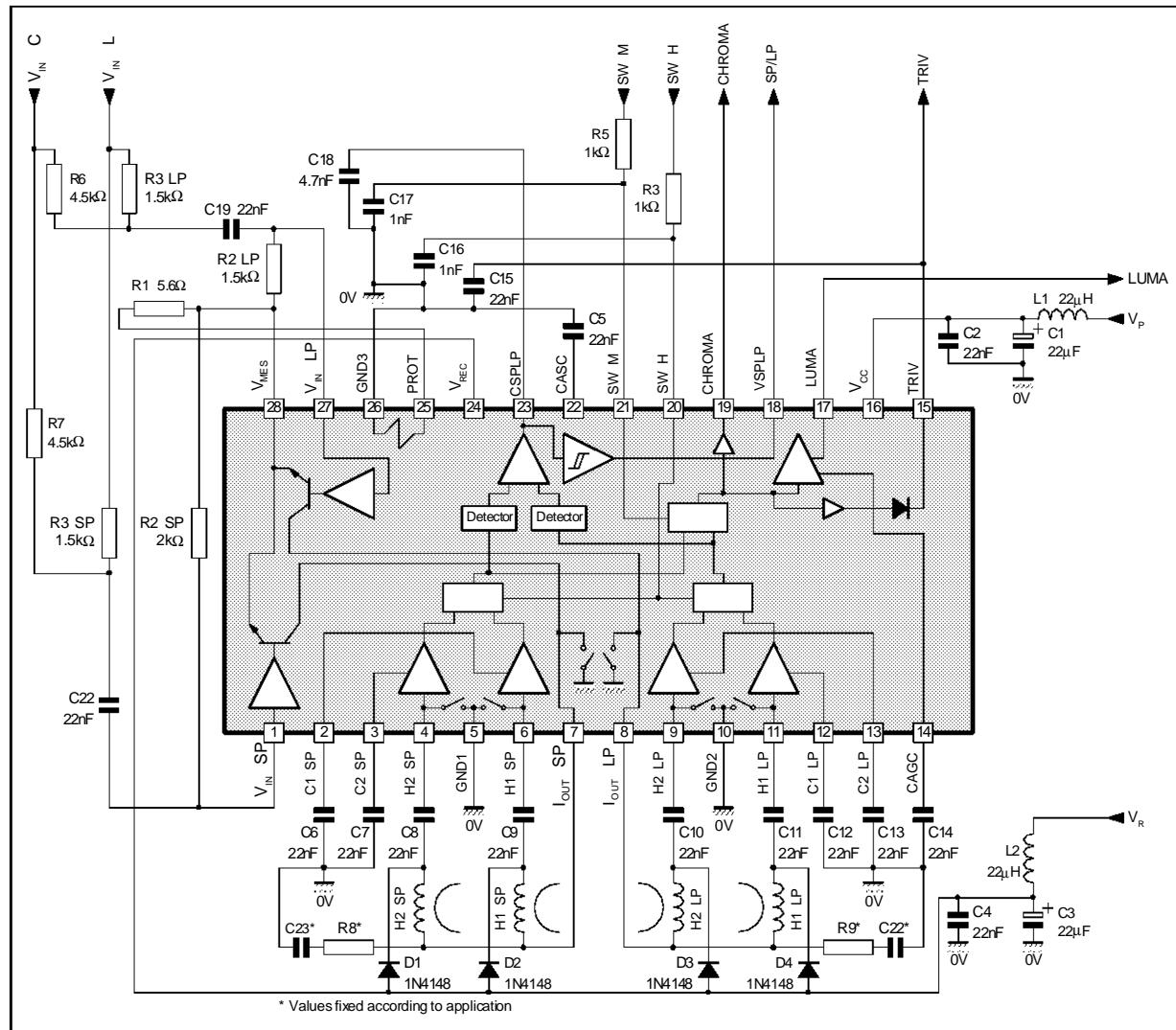
5706A-15.EPS

Pin : VSPLP



5706A-16.EPS

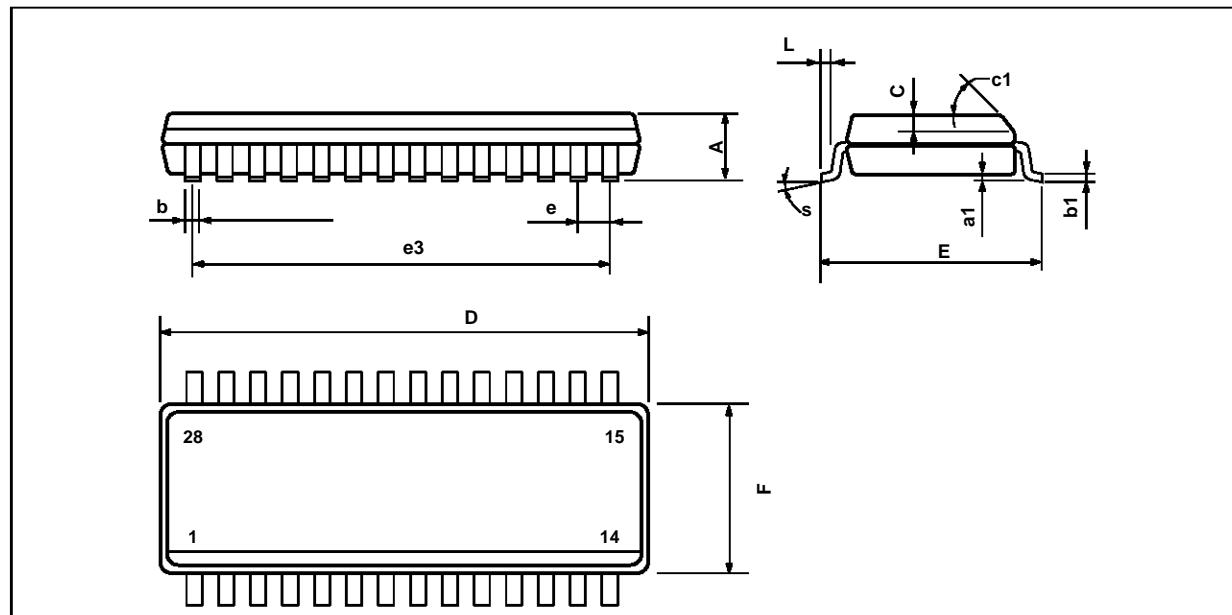
## TYPICAL APPLICATION



5706A-17.EPS

## TEA5706A

### PACKAGE MECHANICAL DATA 28 PINS - PLASTIC MICROPACKAGE



PM-SO28.EPS

SO28.TBL

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1		45° (typ.)				
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S		8° (max.)				

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No licence is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1994 SGS-THOMSON Microelectronics - All Rights Reserved

Purchase of I<sup>2</sup>C Components of SGS-THOMSON Microelectronics, conveys a license under the Philips I<sup>2</sup>C Patent. Rights to use these components in a I<sup>2</sup>C system, is granted provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco  
The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.